

CLAIMS

1 1. An electrostatic discharge (ESD) protective structure that protects an integrated
2 semiconductor circuit connected between a first potential bus with a first supply potential
3 (VCC) and a second potential bus with a second supply potential (VSS), said electrostatic
4 discharge protective structure comprising:

5 a laterally formed electrostatic discharge diode having a first region doped with a
6 first conduction type and a second region, spaced apart from said first region;

7 a doped second conduction type, wherein said electrostatic discharge protective
8 structure is located between the first and second potential busses and drains off an
9 overvoltage pulse to one fo the first and second potential busses, wherein said laterally
10 formed electrostatic discharge diode includes a gate electrode located between said first
11 region and said second region corresponding to the width (W) or the length of the gate
12 electrode.

1 2. The electrostatic discharge protective structure of claim 1, wherein said protective
2 structure includes a semiconductor body having a surface in which said first region and
3 said second region are embedded, wherein said first region is connected via a first
4 electrode to the first potential bus, and said second region is connected via a second
5 electrode to the second potential bus.

1 3. The electrostatic discharge protective structure of claim 2, wherein said
2 semiconductor body includes charge carriers of the second conduction type, and said gate

3 electrode and said second electrode are connected to said second potential bus.

1 4. The electrostatic discharge protective structure of claim 2, wherein said
2 semiconductor body includes charge carriers of the first conduction type, and at least one
3 well of the second conduction type is embedded in said semiconductor body, and said first
4 and second regions are embedded in said well.

1 5. The electrostatic discharge protective structure of claim 4, wherein said second
2 regions laterally enclose said first regions.

1 6. The electrostatic discharge protective structure of claim 4, wherein the integrated
2 semiconductor circuit is configured and arranged as an MOS or CMOS circuit.

1 7. The electrostatic discharge protective structure of claim 2, comprising a gate
2 dielectric that spaces said semiconductor body at a distance from the gate electrode.

1 8. The electrostatic discharge protective structure of claim 7, wherein said gate
2 dielectric contains silicon dioxide and said gate electrode contains polysilicon.

1 9. A method for producing an electrostatic discharge protective structure that is co-
2 integrated into an integrated circuit with a circuit to be protected, and the electrostatic
3 discharge protective circuit and the circuit to be protected are disposed electrically in
4 parallel between first and second voltage busses, said method comprising:

5 inserting doping atoms of a first conduction type for the first region;

6 inserting doping atoms of a second conduction type for the second region;

7 applying a gate dielectric to the first surface over an enrichment region that is
8 located between the first region and the second region;

9 applying a metallization or a polysilicon layer respectively to the first and second
10 regions and to the gate dielectric.

1 10. The method of claim 9, wherein said gate dielectric and said gate electrode are
2 produced first, and then said first and the second regions are inserted in a self-adjusting
3 manner into the semiconductor body using the gate dielectric as a mask.

1 11. The method of claim 10, wherein said step of inserting doping atoms of a first
2 conduction type for the first region includes the step of ion implantation of the doping
3 atoms into the first region.

1 12. The method of claim 10, wherein said integrated semiconductor circuit and said
2 electrostatic diode are produced in MOS/CMOS technology.

1 13. An integrated circuit with electrostatic discharge protection, said integrated circuit
2 comprising:

3 a circuit to be protected;

4 an electrostatic discharge device that is disposed electrically parallel to said circuit
5 to be protected between first and second voltage busses, wherein said electrostatic
6 discharge device includes a laterally shaped electrostatic discharge diode having:

7 (i) a first region doped with a first conduction type material within a

8 substrate;

9 (ii) a second region doped with a second conduction type material within
10 said substrate; and

11 (iii) a gate electrode having a width W and located between said first and
12 second regions such that said first and second regions are separated by the width
13 W .

1 14. The integrated circuit of claim 13, comprising a gate oxide disposed on said
2 substrate between said first and second conduction regions and underlying said gate
3 electrode.

1 15. The integrated circuit of claim 14, comprising a first electrode disposed on said
2 substrate overlaying said first region, and a second electrode disposed on said substrate
3 overlaying said second region, wherein said first electrode is connected to the first voltage
4 bus and said second electrode is connected to said second bus.